Abstract of the disclosure

A circuit defining a second system clock in a system comprising a master connected to one or more slave devices via a channel, the channel communicating an externally generated first system clock towards the master. The circuit comprising a delay locked loop circuit configured to receive the first system clock and a second phase feedback signal as inputs and to generate a transmit clock signal. A 90 degrees block configured to receive the transmit system clock and to generate a 90 degrees phased shifted version of the transmit clock signal. An output driver circuit configured to receive the 90 degrees phased shifted version of the transmit clock signal and to generate the second system clock. A first phase detector configured to receive a receive system clock and the transmit system clock and to generate a first phase feedback signal. A delay element configured to receive the first system clock and the first phase feedback signal and to generate a delayed first system clock. A second phase detector configured to receive the delayed first system clock and the second system clock and to generate the second phase feedback signal.